A DISTRIBUTED MONOLITHIC 2-18 GHZ DUAL-GATE FET MIXER

Thomas S. Howard and Anthony M. Pavio

Texas Instruments Incorporated
P O Box 660246, MS 255
Dallas, Tx 75266

ABSTRACT

A novel broadband mixer topology, which can be implemented using either monolithic or discrete integrated circuit methods, has been developed using distributed design techniques. The MMIC mixer exhibits excellent 2-18 GHz conversion gain performance with signal handling capabilities and LO drive requirements similar to conventional diode double-balanced circuits.

INTRODUCTION

The ever increasing complexity of modern EW receiver systems has placed stringent demands on component size, weight and performance. Thus, it has become very difficult to package amplitude and phase tracking multi-channel receivers with their numerous amplifiers and mixers in the space allotted for typical airborne systems. Monolithic mixers and amplifiers, using GaAs FETs as active elements, help achieve these goals.

THEORY OF OPERATION

Although the use of distributed structures to achieve broadband gain and low VSWR performance has been used to design amplifiers [1, 2, 3], little work has been done in using these techniques to design distributed mixers. The distributed mixer, as explained in reference [4], employs the input capacitance of the FET gates and high impedance series transmission lines to realize a lumped element transmission line section of impedance Z_O. Several dual-gate FETs can be cascaded in this way to form very broadband structures for both the LO and RF mixer ports (Figure 1). Thus, low VSWR on both ports and good LO to RF isolation can be achieved (a result of gate to gate isolation).

These transmission lines must have equal phase shifts between the FET stages when the mixer is operating as a down-converter with a low IF frequency. Equal phase shifts yields a constant phase offset at the IF frequency which allows the IF power to be summed by connecting the drain node of the dual-gate FETs together. Higher IF frequencies, or use of this mixer as an up-converter, would require that the drains of the FETs also be connected with a traveling-wave structure.

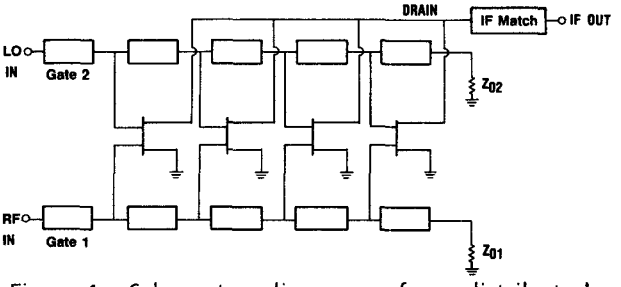

Figure 1. Schematic diagram of a distributed mixer using dual-gate GaAs FETs.

A variety of design considerations, which affect the bandwidth, conversion gain and producibility of the mixer, were analyzed. Some of these considerations were: 1) number of FETs, 2) FET gate periphery, 3) gate resistance, 4) LO power requirements, and 5) monolithic chip area. To obtain a bandwidth that extended to 18 GHz, FETs with 0.5 µm gate lengths were necessary and the total gate periphery needed to be less than 800 µm. The size constraints of the chip and LO drive requirements combined to limit the final design to four 0.5 µm x 150 µm FETs. This FET was modeled as a cascode combination of two single-gate FETs (Figure 2) with the component values adjusted to match the small-signal S-parameters.

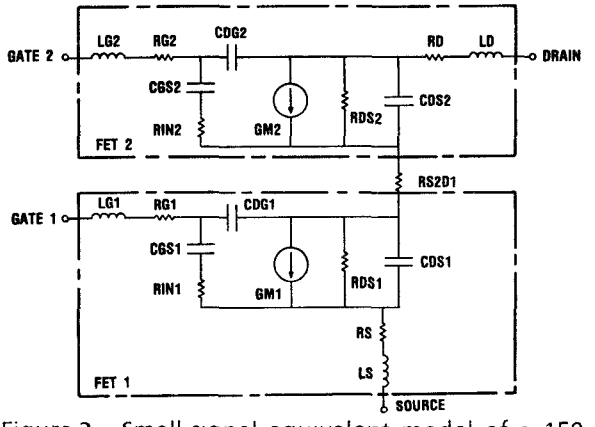

Figure 2. Small-signal equivalent model of a 150 µm dual-gate GaAs FET.

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The circuit was designed using both linear and nonlinear analysis techniques. A linear analysis program was used to optimize the voltages seen at the gate of each FET in order to achieve efficient equally distributed mixing action. After the RF input line was modeled, the phase shift between FETs on the LO line was matched to the RF line. A maximum VSWR of 2:1 across the 2-18 GHz band was the goal for both ports. A nonlinear analysis program, based on the harmonic balance method [5], was used to predict the performance of the FET as a mixing element and to determine the optimum bias conditions. The program inputs include the small-signal model (Figure 2) and the I-V curves shown in Figure 3. The linear, small-signal model is modified by combining the transconductance, g_m, and the output resistance, R_{ds}, into a nonlinear current source which is dependent on the gate-to-source (V_{gs}), and drain-to-source (V_{ds}), voltages. The instantaneous value of the drain current is found from the I-V curves and then converted back to the frequency domain by use of the Fourier transform. The DC bias voltage on gate 2 of the dual-gate FET was found to strongly influence the conversion efficiency of the mixer by establishing the range over which the LO voltage swing occurred. Nonlinear analysis predicted and tests on

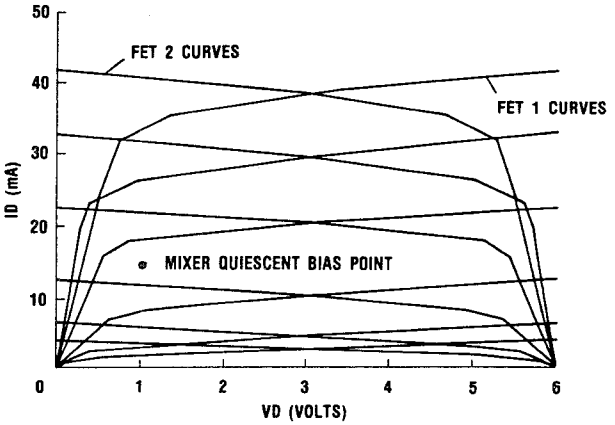

Figure 3. I-V transfer characteristics of a 150 μm dual-gate FET.

simple circuits verified that a gate 2 voltage between -0.5 and 0 volts gave the best conversion gain. Zero volts was used in the design to simplify the DC bias network.

CONSTRUCTION

The monolithic mixer shown in Figure 4 was fabricated on a 0.15 mm thick semi-insulating GaAs substrate that is 1.57 mm wide by 2.54 mm long. The active layer was formed by ion implantation with a low noise profile. Etching the active layer provides isolation between the FETs. Included on the circuit are blocking and bypass capacitors, of the metal/silicon nitride/metal type which have approximately 0.2 μm of dielectric thickness. The resistors on the chip were formed by selective etching of the active layer which yields resistors with a sheet resistivity of 400 ohms per square in their linear region. There is no DC blocking capacitor on the drain output because the low IF frequency would require an extremely large capacitance value.

RESULTS

Two types of mixer circuits were designed and fabricated on the same GaAs wafer to tailor the mixer performance to different applications. The output impedance at the drain node of the mixer (at low IF frequencies) is on the order of 2,000 ohms for each FET for a total impedance of approximately 400 to 500 ohms, which makes a poor match to 50 ohms. The first mixer type employed no IF port matching to enable the characteristics of the mixer alone to be investigated while the second circuit includes a matched IF amplifier on the chip. Excellent conversion gain characteristics were obtained with both designs throughout the entire 2-18 GHz frequency range. A photograph of one of the monolithic circuits is shown in Figure 4 with the IF amplifier visible in the

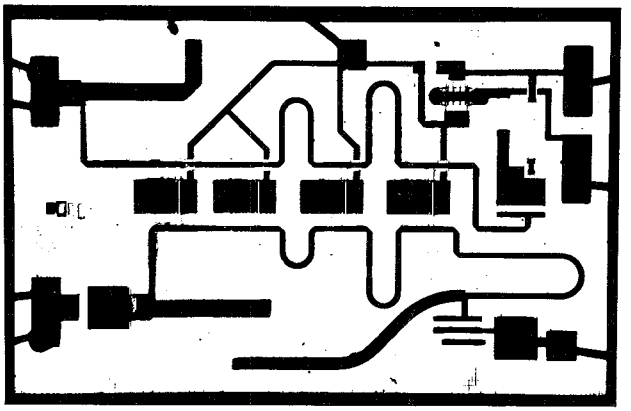

Figure 4. Photograph of the monolithic distributed four stage mixer with integrated IF amplifier.

upper right hand corner of the chip. The conversion gain of the mixer is displayed in Figure 5 with an IF termination of 50 ohms. The dip in the response at 6 GHz is due to a mismatch on the LO port. The impedance seen at the LO port at this frequency is below 50 ohms; this limits the voltage swing at the gate of the FETs and decreases conversion gain. A wide IF bandwidth is obtained

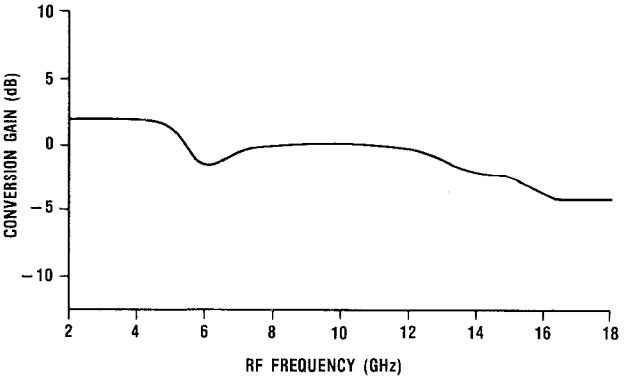

Figure 5. Conversion gain of the distributed mixer at an IF = 500 MHz.

when using a 50 ohm load, as shown in Figure 6, at the expense of maximum conversion gain. The roll-off at the low end of the IF band is caused by the bias network used to provide the FETs with DC current. Both responses shown were obtained with a LO drive level of approximately 10 dBm at an IF frequency of 500 MHz and optimum gate 1 bias voltage. The effect that the gate 1 bias voltage has on conversion efficiency can be seen in Figure 7.

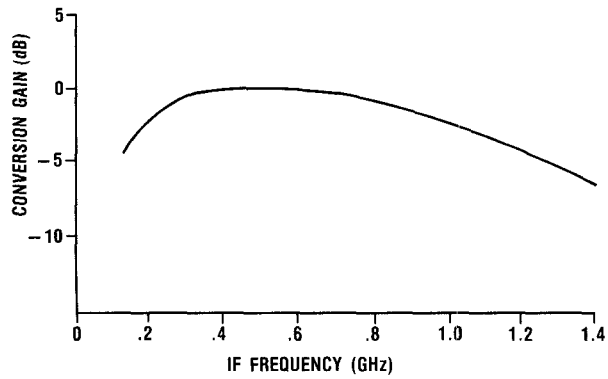

Figure 6. Conversion gain of the mixer as a function of IF frequency.

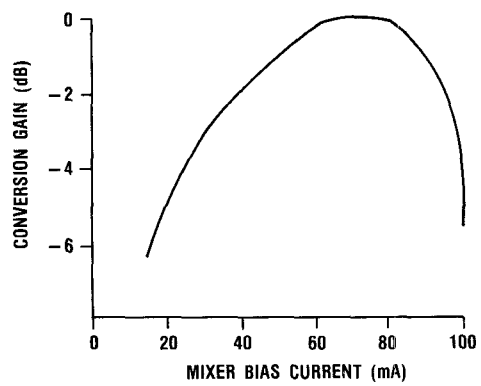

Figure 7. Conversion gain variation versus drain current (gate 1 bias voltage is being varied).

The conversion gain rises at the gate voltage is increased from pinch-off because the gain of the individual FETs is increasing. Then over a fairly broad range of bias levels, the conversion gain is constant indicating that the nonlinear mixing action is insensitive to gate 1 voltage. Finally, as the FET drain current nears its maximum current (V_{gs1} = 0, V_{gs2} constant), the conversion gain drops abruptly because the LO voltage swing is no longer able to drive the FET into its pinch-off region. The FET is then being operated in a linear regime which degrades mixing action. The compression of the RF signal, measured at mid-band, is indicated in Figure 8 with the 1 dB compression point occurring when 4 dBm is applied to the input. The RF and LO port return loss curves are shown in Figures 9 and 10 respectively. The RF port return loss curve responds very closely to the modeled VSWR; however, the LO port return loss doesn't match the model due to its large-signal behavior and the uncertainties in the modeling of the second gate. The LO to RF isolation is typically greater than 23 dB.

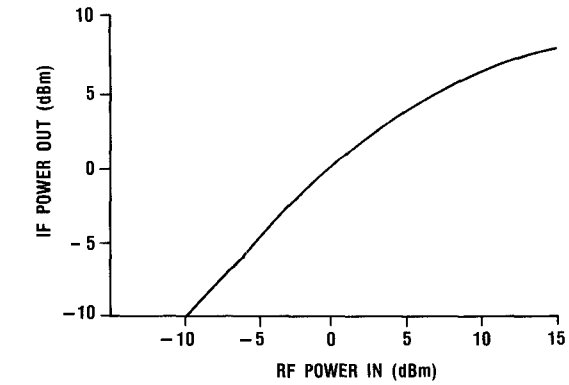

Figure 8. Compression of the RF signal at 10 GHz with a LO drive level of + 10 dBm.

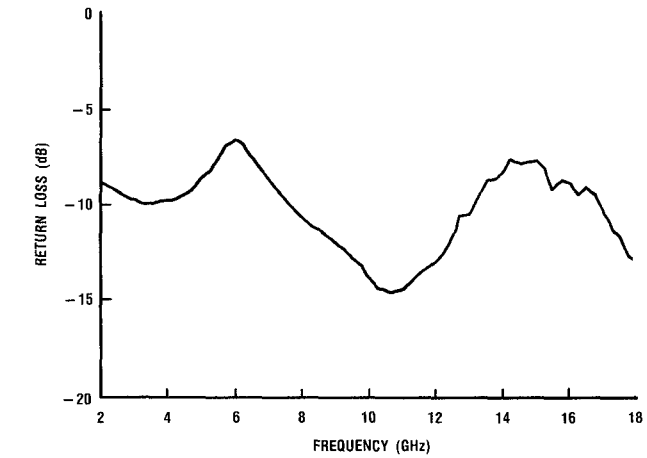

Figure 9. RF port input return loss.

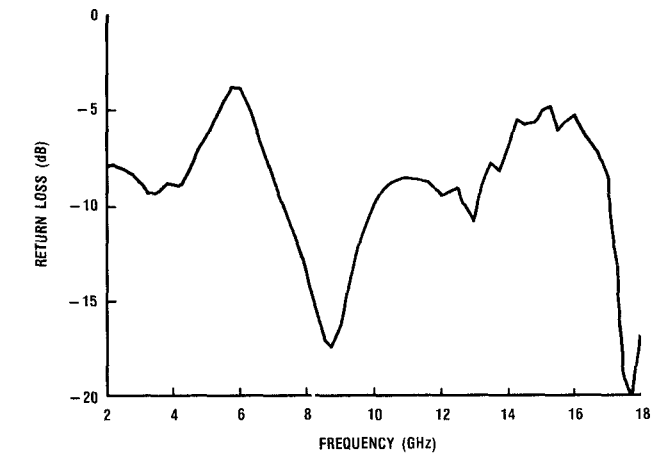

Figure 10. LO port input return loss with 10 dBm applied.

The second mixer circuit employed a 300 µm single-gate FET in a common source feedback amplifier to provide IF matching and gain. To avoid a low frequency cutoff and necessitate a large blocking capacitor, this amplifier was connected directly to the summed drain nodes of the mixer. This action forced the amplifier to be self-biased because the drain voltage of the FETs (5 to 8 volts)

appears on the gate. Both on chip and off chip resistors are used to set the bias point and off chip capacitors shunt the source to ground. To match the 400 ohm mixer IF impedance, shunt resistive feedback was used. The IF bandwidth of this style of mixer is reduced because the gate and drain capacitances and the DC bias network have a greater impact in a high impedance system. The conversion gain response of this circuit is shown in Figure 11 with LO power of 10 dBm at an IF of 400 MHz and optimum mixer bias. The IF amplifier provides 5 to 6 dB gain with the rest of the conversion gain increase coming from an improvement in the IF match. The final graph (Figure 12) displays the response of this circuit to varying LO power. Initially the conversion gain increases dramatically versus the LO power, but then around 10 dBm the response begins to saturate and further increases in the LO level yield smaller gains in conversion efficiency.

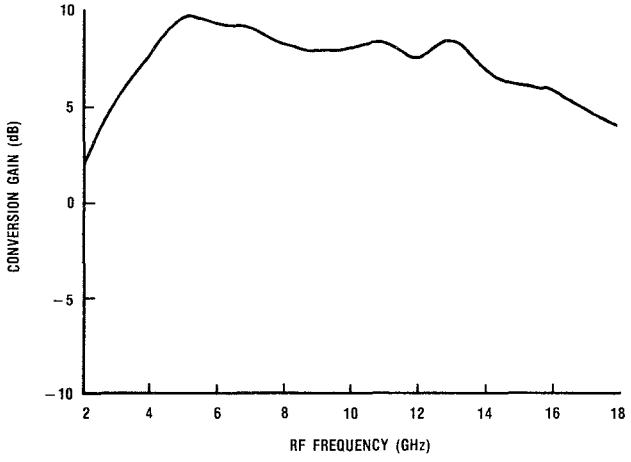

Figure 11. Conversion gain of the mixer/IF amplifier combination at an IF = 400 MHz.

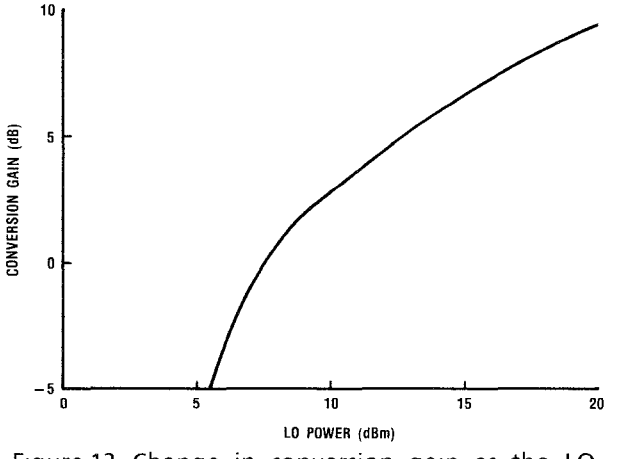

Figure 12. Change in conversion gain as the LO power is varied.

CONCLUSION

Because of the excellent broadband performance demonstrated by these mixers, it is now possible to employ completely monolithic broadband receiver converters in modern EW systems. These receivers can be extremely small and lightweight and maximize the advantages obtained from automated manufacturing methods. With the use of monolithic receiver components and automated assembly techniques, the resulting receivers will also exhibit excellent amplitude and phase tracking performance

REFERENCES

(1) Y. Ayalsi, R. Mozzi, J. Vorhaus, L Reynolds, and R. Pucel, "A Monolithic GaAs 1-13 GHz Traveling-Wave Amplifier", IEEE Trans Microwave Theory Tech , vol. MTT-30, no 7, pp. 976-981, July 1982.

(2) J. Schellenberg, H. Yamasaki, and P. Asher, "2 to 30 GHz Monolithic Distributed Amplifier", 1984 GaAs IC Symposium Digest, pp 77-79.

(3) E. Strid and K. Gleason, "A DC-12 GHz Monolithic GaAs FET Distributed Amplifier", IEEE Trans Microwave Theory Tech., vol MTT-30, no. 7, pp. 969-975, July 1982.

(4) T. Howard and A. Pavio, "A Distributed 1-12 GHz Dual-Gate FET Mixer", 1986 IEEE MTT-S Inter. Microwave Symposium Digest, pp. 329-332.

(5) D. Peterson, A. Pavio, and B Kim, "A GaAs FET Model for Large-Signal Applications", IEEE Trans Microwave Theory Tech., vol MTT-32, no. 3, pp 276-281, March 1984

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